News Release from

DRC RECONFIGURABLE COPROCESSORS GO MAINSTREAM WITH APPLICATIONS RUNNING UP TO 100 TIMES FASTER

FPGA Journal published DRC article details evolution of coprocessors from specialized to CPU peers

Sunnyvale, CA, 27 February 2008 — DRC Computer Corporation (DRC), the leading provider of dynamically reconfigurable coprocessor modules, today announced that FPGA Journal has just published a DRC authored article detailing the benefits and history of reconfigurable computing.

Citing Steve Casselman, DRC CTO and generally recognized as the “Father of Reconfigurable Computing”, the article details how CPU vendors acknowledged that Moore’s Law could no longer deliver enough computing power to satisfy time-critical, data-intense applications like high volume, web based applications and services. AMD was the first to respond opening their HyperTransport bus to coprocessors.

This was the last barrier to coprocessors moving from a specialized niche product to mainstream computing. The DRC coprocessor executes applications at hardware speeds and can therefore achieve accelerations of up to 100 times that of standard commodity CPUs.

The DRC architecture is optimized for applications that require ultra-fast search, sort or encrypt. By deploying a massively parallel on chip architecture applications can execute tens of threads simultaneously.

The full article can be found on the FPGA Journal website at:
http://www.fpgajournal.com/articles_2008/20080226_drc.htm

About DRC Computer Corporation
DRC Computer Corporation is the leading provider of true coprocessors addressing the needs of time-critical, data intense applications in the finance industry, security environments, web companies and biomedical markets. If its about search, sort or encrypt DRC can accelerate applications by up to 100 times. Cofounded in 2004 by Larry Laurich and Steve Casselman DRC is headquartered in Sunnyvale, California. For more information, visit www.drccomputer.com.

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