



Reconfigurable Systems Craft a New Breed of “Soft Appliances” that Deliver Topnotch Performance

January 8, 2007 -- As chip designs migrate down the process roadmap from 130 to 90 to 65nm and beyond, the cost of implementing a system-on-chip (SOC) solution doubles to triples at each smaller process node. For example, at 130-nm a typical high-end design from start to finish might cost about \$8 million, while at 90nm it might cost close to \$20 million, and at 65nm, most estimates peg the cost of a high-end SoC at close to \$45 million.

The higher cost to design and implement a chip at each process node is forcing companies to rethink their SOC development plans since the number of chips sold for each design must be in the millions to keep the amortized development cost per chip to a reasonable level. Aside from the consumer and automotive markets, there are few commercial markets (networking, storage, scientific computing, etc.) that have the volumes to justify the high SOC development costs.

When chip applications, such as specialized accelerators and application unique functions, don't create a demand for millions of chips, a programmable off-the-shelf solution rather than an SOC design may be a more cost-effective and more timely alternative. Such a "soft appliance" can reduce system development cost, shorten the time to market, reduce system maintenance, and provide a simple upgrade path. Today's large field-programmable gate arrays (FPGAs) are at the heart of such systems. The latest generations of FPGAs can now deliver system complexity levels (millions of gates and megabits of memory) and performance levels (over 1 billion integer multiply-accumulate operations/s) that suit them for many of the lower-volume applications that cannot justify the development cost of an SoC solution.

The FPGA reconfigurability lets system designs be easily upgraded or fine-tuned for the application at hand, in many cases, delivering better performance than a general-purpose processor and competitive performance with an ASIC/SOC solution. But an FPGA does not make an entire system. What designers need is a complete configurable, yet standard, platform that lets them create a standard base-level product that, via software, can be configured to specific algorithm acceleration or application requirements.

The recent release of the Torrenza platform concept from Advanced Micro Devices, Inc. is a good example of an off-the-shelf open platform (a dual- or quad-socket Opteron motherboard). In the Torrenza open platform, the company has opened the Opteron CPU interface such that customer-centric accelerators that perform special media processing functions – high-speed floating-point or integer computations, gaming physics calculations, XML operations, etc. – can be plugged into one of the CPU sockets to supplement the other Opteron CPU(s) on the board.

The ability to drop a programmable solution into the Opteron socket is just one example of how future systems can leverage programmable technology to achieve faster time to market and improve system flexibility and performance. The reconfigurable processing unit (RPU) developed by DRC Computer is one of the first of several FPGA-based industry offerings now available as off-the-shelf solutions that can leverage the 940-contact zero-insertion-force sockets on the Torrenza platform to deliver application-optimized acceleration.

The DRC RPU consists of a Xilinx Virtex-4 family FPGA that ranges in capacity from 110,000 to 200,000 logic cells (about 2.5 to 5 million gates of logic) and from 4 to 6Mbits of SRAM. Supporting the FPGA, the RPU also includes sockets for two 1-GByte DDR2 memory modules and 256MBytes of reduced-latency DRAM. Three 8-bit wide Hypertransport interfaces on the module operate at 400MHz and provide direct low-latency high-speed links to the Opteron subsystem on the Torrenza platform. Linux drivers supplied with the RPU allow the host processor to manage the configuration downloads and application interface to the RPU.

Emerging FPGA-based platforms such as the RPU can be loaded (during system boot time or even at any point when the system is operating) with the desired configuration to execute algorithms for any of the previously mentioned applications or yet other tasks. Typical applications that the

programmable engine can handle include network processing for content and security analysis; enterprise applications for database mining, storage management, Java acceleration; media processing such as transcoding, IPTV streaming, and image processing; telecommunications support for voice-over-IP management; and general application support in the form of compute acceleration for graphics and data analysis.

Whether a Torrenza-like platform is a low-cost standard PC or server motherboard, or a server blade, designers can leverage the open interface to plug in a flexible programmable RPU or similar module and then bring their application-specific knowledge to it through configuration software. A reprogrammable solution works well when system volumes can't justify the design of an ASIC to provide the desired solution, or when system turn-around times can't endure the 12 to 24 months it typically takes to develop an ASIC. Such a reprogrammable solution is also future-proof—since the application-centric portion of the system uses an FPGA, the configuration pattern can always be modified to incorporate a more efficient algorithm, add a new function, etc.



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Michael joined DRC in May of 2006 as COO and has extensive experience in reconfigurable technology. Prior to joining DRC, he was the CEO of Veridicom, a Bell Labs spinout company. Before Veridicom, D'Amour was a co-founder and executive vice president of R&D and international operations at Quickturn Design Systems, which offers reconfigurable emulation tools. Previous to that, he was a founding team member vice president of R&D at Daisy Systems Corp. Mr. D'Amour studied engineering at the United States Naval Aviation Technical Training Center and is an active member of IEEE.

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