



## **FPGA-based coprocessors simplify ASIC emulation**

**July 2, 2007** -- With compressed time lines and intense pressure to get it right the first time, ASIC emulation has become an increasingly critical part of the design process. Designers have historically had few good options for emulating ASICs, however. Now, many are turning to a new tool: FPGA-based coprocessors. These reconfigurable coprocessors are allowing designers to eliminate many of the issues associated with conventional ASIC emulation and deliver more accurate designs more quickly and with less effort.

A coprocessor approach also allows for much faster startup times than building hardware from scratch. In addition, because the reconfigurable processor has a tightly coupled, low-latency link with the CPU, designers can exercise the emulated hardware they create at very high speeds--orders of magnitude faster than a software simulator.

A reconfigurable coprocessor also more closely models the real environment in which the ASIC will operate. Running the emulation with an FPGA forces designers to use more deliberate design rules than they might employ when simulating with software. If the code runs well on the FPGA, it will run well in the ASIC.

To illustrate, assume the designer is working with a high-volume chip manufacturer that wants to add MPEG-4 video functionality to an existing ASIC design to enable new video features in portable media devices and cell phones. This example presents a number of inherent challenges. MPEG-4 functionality will require the ASIC to perform some relatively complex algorithmic functions, resulting in the need for in-depth verification--at both the logic and the algorithmic levels.

While the designer only needs to test a few MPEG-4-specific functions--a small addition to the previous generation of the ASIC--the build-your-own hardware approach requires a new printed-circuit board to run them on. Even when beginning with a complete design and schematics, the board design and manufacture is likely to take a month or more.

The designer also will need to build the environment in which the FPGA will operate and debug all of those interfaces, as well as the pc board, even beginning to look at the algorithm. To simulate the relatively complex algorithms involved in MPEG-4 transforms, the team will also need members with advanced skills in the programming-language interface.

With a reconfigurable coprocessor, the simulation environment is already created and all of the interfaces are well-established and debugged. All of the resources the design team may need--FIFOs, dual-port RAMs and interfaces with larger blocks of memory off-chip--are easily accessible and well-documented. In addition, the interface between the simulated hardware running the logic and the high-level software verifying it against the algorithm is not an issue. The software and the hardware run completely in their own separate environments, and the reconfigurable processor includes a software application interface with a set of easily understood calls to transfer data between the two.

The design runs at 200 MHz, so the team can run simulations in a matter of hours, instead of days or weeks. Ultimately, the team is able to run real RTL in real hardware, at close to speed, and perform all the test cases it needs.

### **By Richard Povey, DRC Computer Corporation**

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