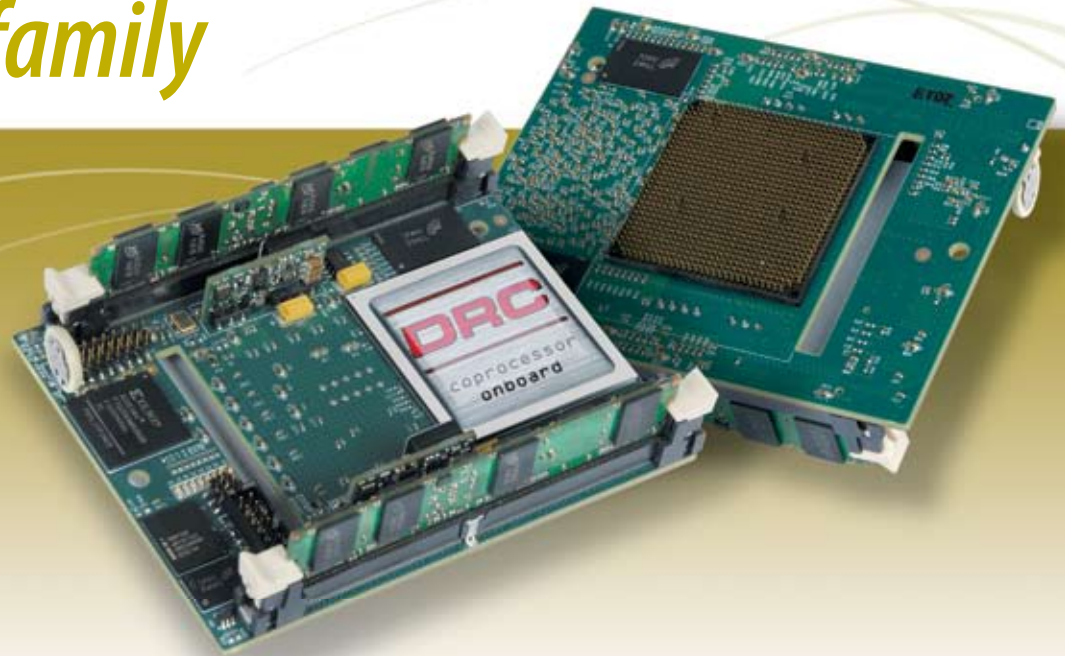


# DRC Reconfigurable Processor Unit



## RPU110 family



### APPLICATIONS

- ▶ modeling
- ▶ simulation
- ▶ rendering
- ▶ synthesis
- ▶ search/sequencing
  - ▶ sorting
- ▶ cryptography
- ▶ compression

### MARKETS

- ▶ geoscience
  - ▶ pharma
  - ▶ defense
    - ▶ CAD
  - ▶ aerospace
- ▶ government
  - ▶ finance
- ▶ entertainment
  - ▶ biotech

## *A memory-rich solution for accelerating your most computationally-demanding applications*

DRC introduces the fastest family of Reconfigurable Processor Unit (RPU) systems on the market today. The DRC RPU110 features an innovative logic array and exceptional bus and memory bandwidth that combine to provide sustainable acceleration for your most challenging supercomputing applications.

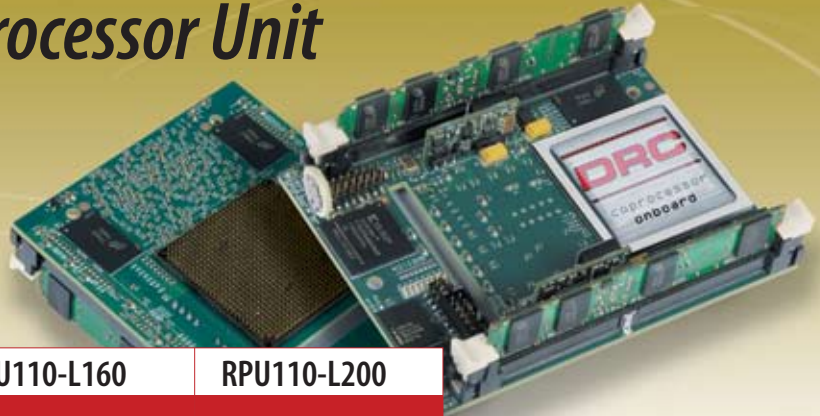
Implementation requires no modifications to workstation or server motherboards. The RPU inserts directly into an open 940 socket in a standard multi-processor AMD Opteron™ system and enjoys direct access to adjacent DDR memory and Opteron processors at HyperTransport™ speed and nanosecond latency. Tight coupling between CPU and memory means that traditional bandwidth and latency bottlenecks are virtually eliminated.

Features of the DRC RPU110 family include:

- ▶ The largest FPGAs on the market
- ▶ On-board RPU memory for total bandwidth of 14.4 GB/second
- ▶ Up to 3 HyperTransport bus interfaces per RPU enabling double the bandwidth using 2 HT buses between 2 CPUs, and supporting expansion to 4-way or larger

*The RPU110 family of DRC RPUs is perfect for large, scalable clusters—dramatically increasing performance and efficiency while reducing costs.*

# DRC Reconfigurable Processor Unit RPU110 family



## TECHNICAL SPECIFICATIONS

	RPU110-L100	RPU110-L160	RPU110-L200
<b>FPGA</b>			
Xilinx Virtex™-4	LX 100	LX 160	LX 200
Number of LUTs	110,592	152,064	200,448
RPU Hardware OS use of LUTs (%): max = HT x 3 plus DDR2 mem ctrl x 2	min 14,400 (13%) max 20,000 (18%)	min 14,400 (9%) max 20,000 (13%)	min 14,400 (7%) max 20,000 (10%)
Memory (BRAM w/ ECC)	240 x 18 kbits	288 x 18 kbits	336 x 18 kbits
<b>Physical/Mechanical</b>			
Socket	940 ZIF	940 ZIF	940 ZIF
Dimensions (mm)	78.7 x 96.5 x 27.9	78.7 x 96.5 x 27.9	78.7 x 96.5 x 27.9
Power dissipation	10-40 W	10-40 W	10-40 W
HT interface	Bus 0, 1, 2	Bus 0, 1, 2	Bus 0, 1, 2
RPU RLDRAM	128 MB	128 MB	128 MB
RPU DDR2 memory	2 x .5 or 1 GB	2 x .5 or 1 GB	2 x .5 or 1 GB
<b>Performance</b>			
HT bus per connection aggregate	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec
Memory (motherboard)	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec
Memory (RPU RLDRAM) per connection aggregate	16 bit DDR 400 800 MB/sec 1.6 GB/sec	16 bit DDR 400 800 MB/sec 1.6 GB/sec	16 bit DDR 400 800 MB/sec 1.6 GB/sec
Memory (RPU DDR2) per connection aggregate	64 bit DDR 400 3.2 GB/sec 6.4 GB/sec	64 bit DDR 400 3.2 GB/sec 6.4 GB/sec	64 bit DDR 400 3.2 GB/sec 6.4 GB/sec
<b>Software/Firmware</b>			
<ul style="list-style-type: none"> <li>▶ Linux Drivers</li> <li>▶ Linux RPU manager</li> <li>▶ HT interface(s)</li> <li>▶ RPU API</li> </ul>	<ul style="list-style-type: none"> <li>▶ RPU Hardware OS                             <ul style="list-style-type: none"> <li>- DDR1/DDR2 memory controller</li> <li>- RPU RLDRAM controller</li> <li>- HT interface(s)</li> <li>- RPU Hardware OS API</li> </ul> </li> </ul>		

## The DRC Development System

DRC also offers a development platform for modifying application subroutines to run in hardware. A DRC Development System is a complete server that includes the DRC coprocessor of your choice and optional software compilation technologies—everything you need for a complete programming environment.



## DEVELOPMENT ENVIRONMENT PARTNERS



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