



APPLICATIONS

- modeling
- simulation
- rendering
- synthesis
- searching/sequencing
 - sorting
- cryptography
- compression

MARKETS

- geoscience
 - pharma
 - defense
 - CAD
- aerospace
- government
 - finance
- entertainment

DRC Reconfigurable Processor Unit

A memory-rich solution for accelerating your most computationally-demanding applications

DRC introduces the fastest family of Reconfigurable Processor Unit (RPU™) systems on the market today. The DRC RPU110 features an innovative logic array and exceptional bus and memory bandwidth that combine to provide sustainable acceleration for your most challenging super-computing applications.

The DRC RPU system dramatically increases performance and efficiency while reducing costs. Implementation requires no modifications to workstation or server motherboards. The RPU inserts directly into an open 940 socket in a standard multi-processor AMD Opteron™ system and enjoys direct access to adjacent DDR memory and Opteron processors at HyperTransport™ speed and nanosecond latency. Tight coupling between CPU and memory means that traditional bandwidth and latency bottlenecks are virtually eliminated.

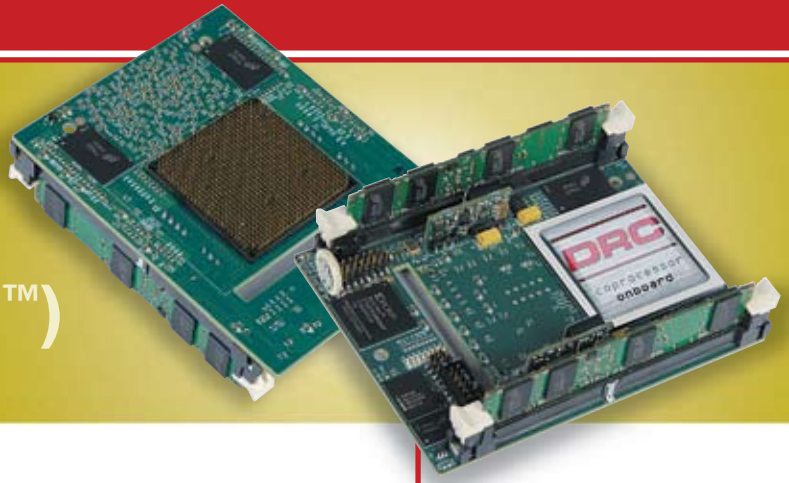
Features of the DRC RPU110 family include:

- The largest FPGAs on the market: Xilinx Virtex™-4 LX 100, Virtex-4 LX 160, or Virtex-4 LX 200.
- On-board RPU memory for total bandwidth of 14.4 GB/second.
- Up to 3 HyperTransport bus interfaces per RPU enabling double the bandwidth using 2 HT buses between 2 CPUs, and supporting expansion to 4-way or larger.

The power and performance advantages of these features are readily realized in most HPC environments. The DRC RPU110 family includes three RPU models defined by the size of FPGA. The RPU110 is perfect for large, scalable clusters, for your most computationally-intensive problems.

RPU110

DRC Reconfigurable Processor Unit (RPU™)



The DRC Reconfigurable Processor Unit

The RPU leverages the features and benefits of AMD64's Direct Connect Architecture and HyperTransport technology to deliver 10-100x performance improvements in many CPU-intensive applications and markets.

RPU110 Family Technical Specifications

	RPU110-L100	RPU110-L160	RPU110-L200
FPGA			
Xilinx Virtex™-4	LX 100	LX 160	LX 200
Number of LUTs	110,592	152,064	200,448
RPSysCore use of LUTs (%)	min 14,400 (13%) max 20,000 (18%)	min 14,400 (9%) max 20,000 (13%)	min 14,400 (7%) max 20,000 (10%)
max = HT x 3 plus DDR2 memory ctrl x 2			
Memory (BRAM w/ ECC)	240 x 18 kbits	288 x 18 kbits	336 x 18 kbits
Physical/Mechanical			
Socket	940 ZIF	940 ZIF	940 ZIF
Dimensions (mm)	78.7 x 96.5 x 27.9	78.7 x 96.5 x 27.9	78.7 x 96.5 x 27.9
Power dissipation	10-40	10-40	10-40
HT interface	Bus 0, 1, 2	Bus 0, 1, 2	Bus 0, 1, 2
RPU RLDRAM	256 MB	256 MB	256 MB
RPU DDR2 memory	2 x .5 or 1 GB	2 x .5 or 1 GB	2 x .5 or 1 GB
Performance			
HT bus per connection aggregate	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec
Memory (motherboard)	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec
Memory (RPU RLDRAM) per connection aggregate	6.4 GB/sec 800 MB/sec 1.6 GB/sec	6.4 GB/sec 800 MB/sec 1.6 GB/sec	6.4 GB/sec 800 MB/sec 1.6 GB/sec
Memory (RPU DDR2) per connection aggregate	2.4 GB/sec 4.25 GB/sec 8.5 GB/sec	2.4 GB/sec 4.25 GB/sec 8.5 GB/sec	2.4 GB/sec 4.25 GB/sec 8.5 GB/sec
Software/Firmware			
<ul style="list-style-type: none"> ■ Linux Drivers ■ Linux RPU manager 	<ul style="list-style-type: none"> ■ RPSyscore - DDR memory controller 	<ul style="list-style-type: none"> - RPU SRAM controller - HT interface(s) - RPSyscore API 	<ul style="list-style-type: none"> ■ HT interface(s) ■ RPSyscore API

The DRC Development System

DRC also offers a development platform for modifying application subroutines to run in hardware. A DRC Development System is a complete server that includes the DRC coprocessor of your choice and optional software compilation technologies—everything you need for a complete programming environment.



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DRC DEVELOPMENT ENVIRONMENT PARTNERS



DRC Computer Corporation
1178 Bordeaux Drive
Sunnyvale, CA 94089
Phone: 408-400-9500
Fax: 408-400-9505