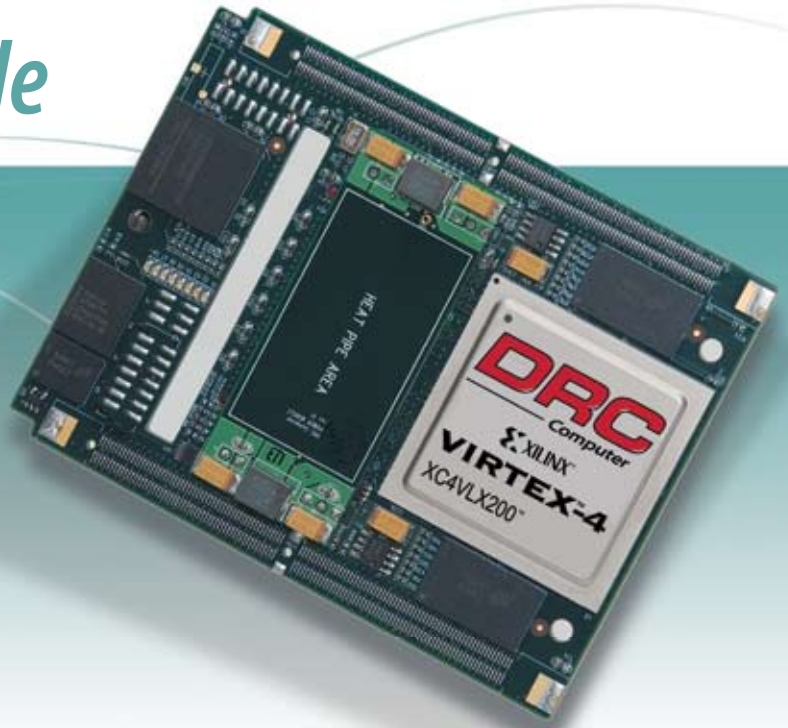


DRC Reconfigurable Processor Unit



RPU110 Low Profile



APPLICATIONS

- ▶ modeling
- ▶ simulation
- ▶ rendering
- ▶ synthesis
- ▶ search/sequencing
 - ▶ sorting
- ▶ cryptography
- ▶ compression

MARKETS

- ▶ geoscience
 - ▶ pharma
 - ▶ defense
 - ▶ CAD
 - ▶ aerospace
- ▶ government
 - ▶ finance
- ▶ entertainment
 - ▶ biotech

A computationally powerful solution for your most demanding applications

The DRC RPU110 Low Profile features an innovative logic array and exceptional bus and memory bandwidth that combine to provide sustainable acceleration for your most challenging supercomputing applications.

The RPU inserts directly into an open 940 socket in a standard multi-processor AMD Opteron™ system and enjoys direct access to adjacent DDR memory and Opteron processors at HyperTransport™ speed and nanosecond latency. Tight coupling between CPU and memory means that traditional bandwidth and latency bottlenecks are virtually eliminated.

Features include:

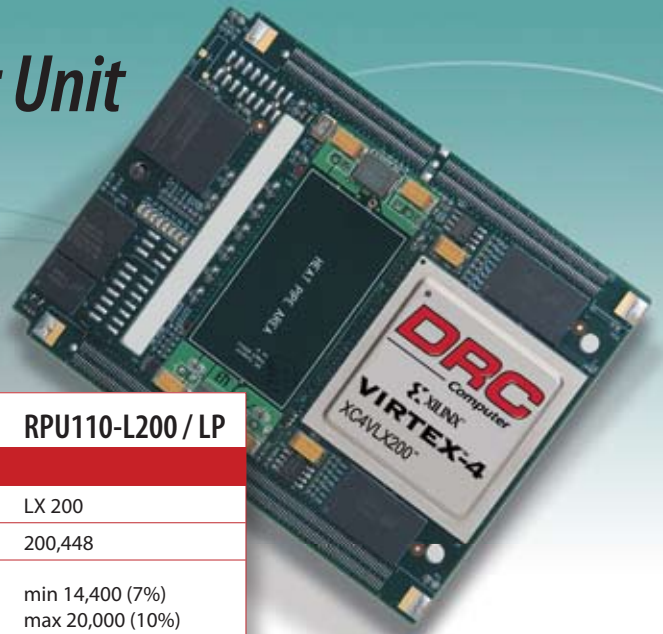
- ▶ The largest FPGA on the market
- ▶ Up to 3 HyperTransport bus interfaces per RPU enabling double the bandwidth using 2 HT buses between 2 CPUs, and supporting expansion to 4-way or larger

The power and performance advantages realized by the RPU110/LP are apparent in most HPC applications. Increased logic resources provide more results per clock cycle, and when combined with greater bus and memory bandwidth the system is balanced to provide real and sustainable application performance.

No modifications to workstation or server motherboards required!

DRC Reconfigurable Processor Unit

RPU110 Low Profile



TECHNICAL SPECIFICATIONS

	RPU110-L100 / LP	RPU110-L160 / LP	RPU110-L200 / LP
FPGA			
Xilinx Virtex™-4	LX 100	LX 160	LX 200
Number of LUTs	110,592	152,064	200,448
RPU Hardware OS use of LUTs (%): max = HT x 3 plus DDR2 mem ctrl x 2	min 14,400 (13%) max 20,000 (18%)	min 14,400 (9%) max 20,000 (13%)	min 14,400 (7%) max 20,000 (10%)
Memory (BRAM w/ ECC)	240 x 18 kbits	288 x 18 kbits	336 x 18 kbits
Physical/Mechanical			
Socket	940 ZIF	940 ZIF	940 ZIF
Dimensions (mm)	78.7 x 96.5 x 10.0*	78.7 x 96.5 x 10.0*	78.7 x 96.5 x 10.0*
Power dissipation	10-40 W	10-40 W	10-40 W
HT interface	Bus 0, 1, 2	Bus 0, 1, 2	Bus 0, 1, 2
RPU RLDRAM	128 MB	128 MB	128 MB
Performance			
HT bus per connection aggregate	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec
Memory (motherboard)	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec	128 bit DDR 400 6.4 GB/sec
Memory (RPU RLDRAM) per connection aggregate	16 bit DDR 400 800 MB/sec 1.6 GB/sec	16 bit DDR 400 800 MB/sec 1.6 GB/sec	16 bit DDR 400 800 MB/sec 1.6 GB/sec
Software/Firmware			
<ul style="list-style-type: none"> ▶ Linux Drivers ▶ Linux RPU manager ▶ HT interface(s) ▶ RPU API 	<ul style="list-style-type: none"> ▶ RPU Hardware OS <ul style="list-style-type: none"> - DDR1 memory controller - RPU RLDRAM controller - HT interface(s) - RPU Hardware OS API 		

* Dimensions shown without heat sink. Heat sink is required for operation.

DEVELOPMENT ENVIRONMENT PARTNERS



The DRC Development System

DRC also offers a development platform for modifying application subroutines to run in hardware. A DRC Development System is a complete server that includes a two-way motherboard, DDR memory, disk drive, and graphics controller. It also includes the DRC coprocessor of your choice and optional software compilation technologies—everything you need for a complete programming environment.

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