

RPU100-L60



APPLICATIONS

- modeling
- simulation
- rendering
- synthesis
- searching/sequencing
 - sorting
- cryptography
- compression

MARKETS

- geoscience
 - pharma
 - defense
 - CAD
 - aerospace
- government
 - finance
- entertainment

DRC Reconfigurable Processor Unit

A breakthrough in coprocessor technology

DRC introduces the patented Reconfigurable Processor Unit (RPU™), a breakthrough coprocessing solution designed specifically for AMD Opteron™ systems. DRC has invented a simple, elegant way to directly connect an FPGA to a processor bus and system memory using a modular RPU that plugs directly into an Opteron socket.

The DRC RPU system dramatically increases performance and efficiency while reducing costs. Implementation requires no modifications to workstation or server motherboards—the RPU inserts directly into an open 940 socket in a standard multi-processor Opteron system and enjoys direct access to adjacent DDR memory and Opteron processors at HyperTransport™ speed and nanosecond latency. Tight coupling between CPU and memory means that traditional bandwidth and latency bottlenecks are virtually eliminated.

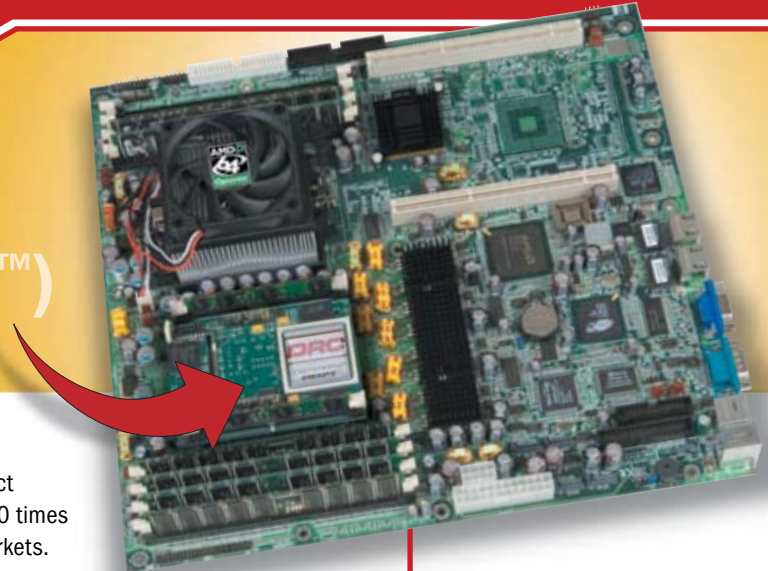
Application acceleration is achieved by offloading the most CPU-intensive and specialized software subroutines to hardware. The DRC RPU enables applications to run many times faster than they would with ordinary acceleration products that connect to a peripheral bus.

The DRC RPU100-L60 model is the most economical acceleration solution DRC offers. It's perfect for your most specific, targeted application acceleration needs where you're seeking maximum efficiency for the price.

DRC
Computer

RPU100-L60

DRC Reconfigurable Processor Unit (RPU™)



The DRC Reconfigurable Processor Unit

The DRC RPU leverages all of the features and benefits of AMD64's Direct Connect Architecture and HyperTransport technology to deliver 10 to 100 times performance improvements in many CPU-intensive applications and markets.

RPU100-L60 Technical Specifications

Physical/Mechanical

- Socket 940 ZIF
- Dimensions (mm) 54 x 50.8 x 9.6
- Power dissipation 5-20
- HT interface Bus 0
- SRAM 512K x 36

Performance

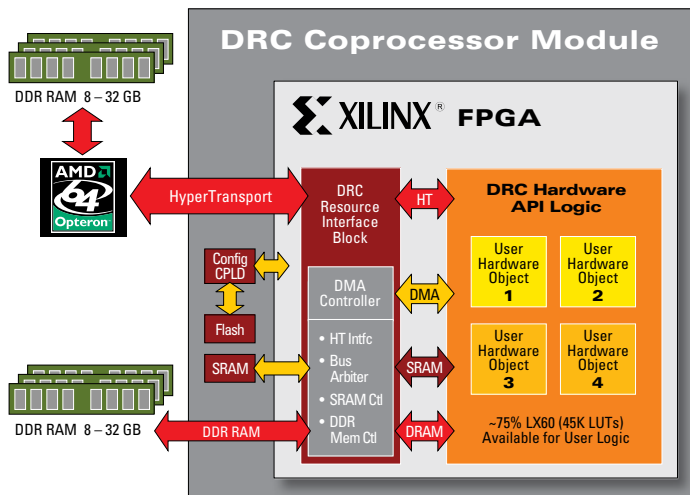
- HT bus (per connection) 400MHz x 8 bits
1.6 GB/sec
- Memory (motherboard) 128 bit DDR 400
6.4 GB/sec
- Memory (RPU SRAM) 800 MB/sec

FPGA

- Xilinx Virtex™-4 LX 60
- Number of LUTs 59,904
- RPSyscore use of LUTs 14,000 (23%)
- Memory (BRAM w/ ECC) 160 x 18 kbits

Software/Firmware

- Linux Drivers
- Linux RPU manager
- RPSyscore
 - HT interface(s)
 - DDR memory controller
 - RPU SRAM controller
 - RPSyscore API



The RPU100-L60 logic flow architecture enables tight coupling between the RPU and motherboard resources.

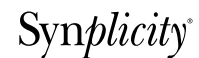
The DRC Development System

DRC also offers a development platform for modifying application subroutines to run in hardware. A DRC Development System is a server containing a two-way motherboard, DDR memory, disk drives, graphics controller and the DRC coprocessor of your choice. Options include pre-configured software compilation technologies—everything you need for a complete programming environment.



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