



Accelium™ Coprocessors



Accelium Coprocessor

Delivering ultra-high throughput, very low latency and massive memory addressability the DRC Accelium coprocessor supports the most demanding of applications. Accelium fits into a standard AMD Opteron™ Socket F slot and supports the AMD Direct Connect Architecture providing very low latency transfers directly to motherboard memory unencumbered by intermediate memory controllers.

The Accelium coprocessor consists of 4 onboard low latency memory systems as well as direct access to the motherboard memory, the largest FPGA commercially available and support for 3 interprocessor busses. Specifically Accelium delivers:

- Total memory support of 20.5GB rising to 68.5GB with high density DRAM
- Internal memory bandwidth in excess of 1 TB/s
- External memory bandwidth of 15 GB/s
- 300 nanosecond latency
- Very low power with maximum consumption of 40 watts
- Xilinx Virtex™-5 FPGA with up to 330,000 logic cells and 576 x 18 kbits Block RAMs

The DRC Accelium coprocessor is a patented, ultra-high performance engine that executes complex data manipulation routines up to 100 times, or more, faster than software equivalents.

These coprocessor routines are available to co-resident x86 based applications through the DRC API and require no source code changes to the application.

Tightly coupling the Accelium coprocessor with a CPU delivers very low latency, ultra-high data bandwidth to the most demanding applications. Architected for applications that are sub-second time-critical and/or that process giga-bytes of data the Accelium coprocessor delivers unprecedented performance.

Accelium uses process pipelining and replication in its massively parallel architecture. Further advantages are achieved with the ability to right-size operators to any data width and to utilize multi-input operators, frequently reducing iterative processes to single cycle operations.

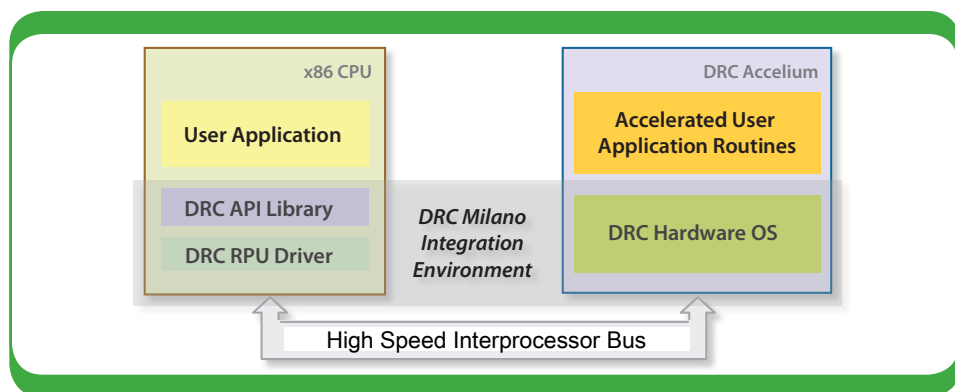
The DRC Milano hardware operating system integrates the Accelium

coprocessor with the x86 CPU to provide a user friendly application support environment. Milano is a sophisticated, low overhead operating system.

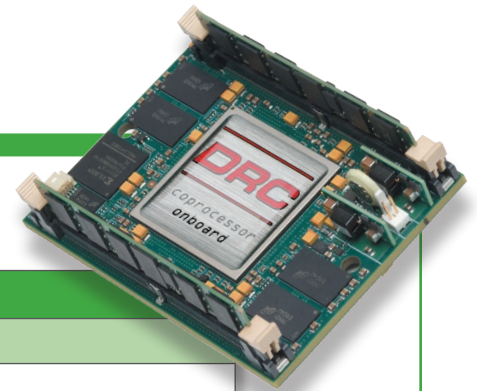
Milano™ Integration Environment

Milano™ is a set of DRC services that seamlessly integrates the DRC RPU with the x86 CPU. With API, driver and management interface on the CPU, and a hardware operating system on the DRC RPU the following realtime functions are provided:

- DMA and interprocessor arbitration management
- Very low overhead and low latency paths
- Coprocessor resource arbitration management
- Run Time Reconfiguration
- In-field upgradeable
- Set of well behaved, consistent interfaces
- Full Linux support



Accelium 2000 Coprocessor Model Specifications



Accelium Model	AC2020	AC2030
FPGA		
Xilinx Virtex™-5	LX 220	LX 330
Number of LCs	207,360	330,000
Memory (BRAM w/ ECC)	354 x 18 kbits	576 x 18 kbits
Hardware OS utilization		
LCs	Max 36,500	Max 36,500
BRAMs	Max 110	Max 110
Physical/ Mechanical		
Socket	1207 LGA	1207 LGA
Dimensions (mm)	76.2 x 101.6 x 27.9	76.2 x 101.6 x 27.9
Power dissipation (watts)	10-40	10-40
Interprocessor bus	Bus 0, 1	Bus 0, 1, 2
Coprocessor memory		
RLDRAM	256 MB	512 MB
DDR2 — optional	None	2 x 2 GB
Performance		
Interprocessor bus per connection aggregate	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec	400MHz x 16 bits 3.2 GB/sec 9.6 GB/sec
Memory (motherboard)	2 x 64 bit DDR 400 6.4 GB/sec	2 x 64 bit DDR 400 6.4 GB/sec
Memory (RPU RLDRAM) per connection aggregate	2 x 16 bit DDR 400 800 MB/sec 1.6 GB/sec	2 x 32 bit DDR 400 1.6 GB/sec 3.2 GB/sec
Memory (RPU DDR) per connection aggregate	N/A	64 bit DDR 400 3.2 GB/sec 6.4 GB/sec

Specifications are subject to change without notice.



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